RX5 Pentusa Base Station

RX5 Overview

The RX5 Pentusa is a powerful multiple DSP device well suited for processing high channel count neurophysiology data in real-time. A streamlined hardware interface provides connections to up to 64 channels for neurophysiological data acquisition.

The RX5 is equipped with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs and serves as a base station for up to four Medusa preamplifiers to form a powerful multi-channel amplifier system. The multiprocessor architecture provides simultaneous ~25 kHz sampling on every channel, 16-bit precision, fiber optic isolation, and the power of user-programmable real-time DSPs.

The RX5 also features front panel status indicators, 40 bits of configurable digital I/O, and four D/A converters for versatile experiment control and stimulus generation.

Power and Communication

The RX5 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

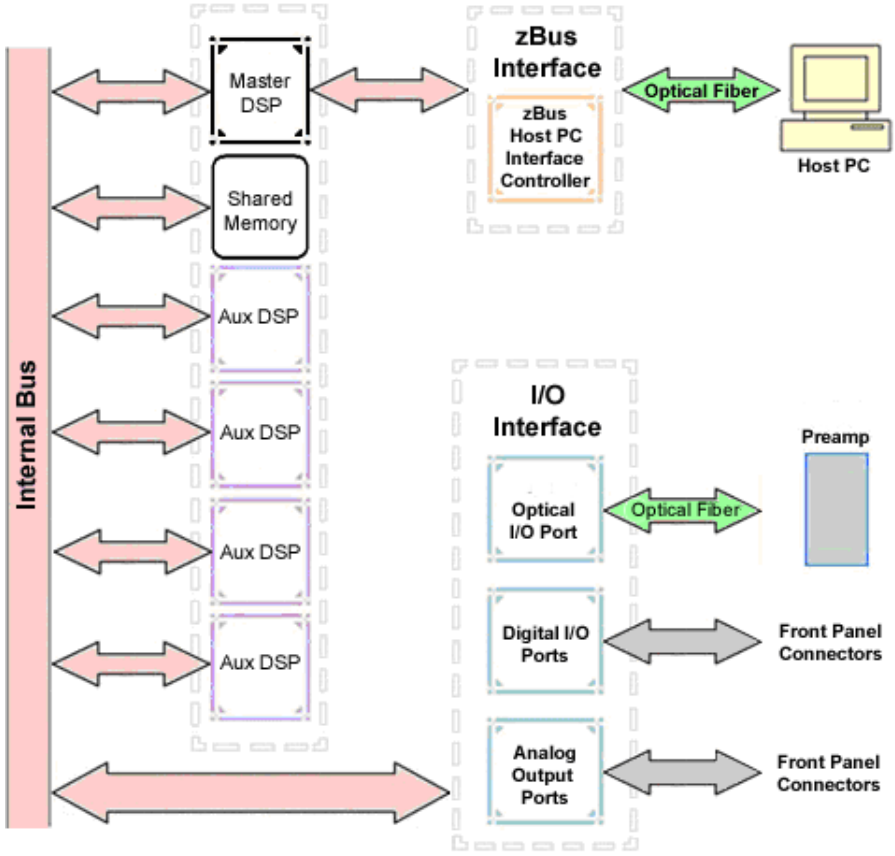
RX Architecture

Each RX multiprocessor device is equipped with either two or five digital signal processors (DSPs). The multi-DSP architecture allows processing tasks to be

distributed across multiple processors and enables data to be transferred to the PC quickly and efficiently. The DSPs include one master and one or four auxiliary DSP(s). 128 MB SDRAM of system memory is shared by all DSPs. When designing circuits the maximum number of components for each RX DSP is 256.

Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

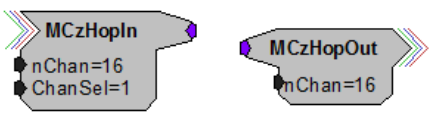
Because the zBus communicates only with the master processor, these devices operate most efficiently when the circuit related processing tasks assigned to the master DSP are minimized, allowing more processor power (cycles) for communication and overhead tasks.

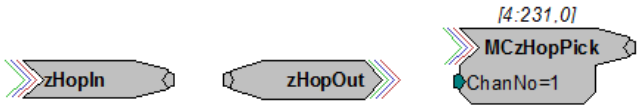


The RX5 contains two DB25 connectors for interfacing with 40 bits of digital I/O and 4 channels of analog output. A BNC connector is provided for access to the first analog output channel. Four fiber optic Medusa preamp ports enable connections for up to 64 channels of analog input.

Distributing Data Across DSPs

In RPvdsEx data can be transferred between each of the auxiliary DSPs as well as the master DSP using zHop components.





Components such as MCzHopIn and MCzHopOut can be used for multi-channel signals while components such as zHopIn, zHopOut, and MCzHopPick are used with single-channel signals. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop Bus introduces a single sample delay. However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

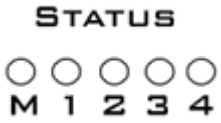
See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX5 Features

DSP Status Displays

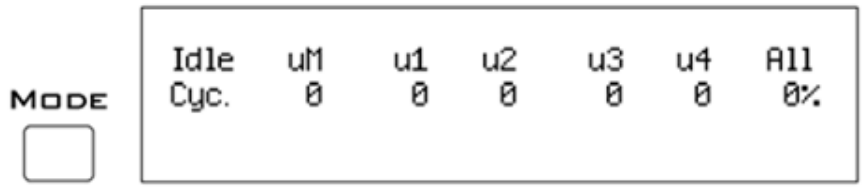
All high performance RX multiprocessors include status lights and a VFD (Vacuum Fluorescent Display) screen to report the status of the individual processors.

Status Lights



Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash rapidly (~3 times per second).

Front Panel VFD Screen



The front panel VFD screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run! or Idle, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The VFD screen may also report system status such as

booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

Cyc:	cycle usage
Ovr:	processor cycle overages
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Fiber Optic Ports

The RX5 base station acquires digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier and the base station. Two or four fiber optic ports are provided to support simultaneous acquisition from up to four preamplifiers. Each port can input up to 16 channels at a maximum sampling rate of ~25 kHz. The first two ports provide oversampling. See "Fiber Oversampling", below for more information.

The fiber optic ports can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A	1 – 16
Amp-B	17 – 32
Amp-C	33 – 48
Amp-D	49 - 64

Fiber Oversampling

The fiber optic cable that carries the signals to the fiber optic input ports has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sample rate of 24.414 kHz.

However, the need may arise to run a circuit at a higher sample rate while still acquiring data via a fiber optic port. The first two fiber optic ports can oversample the digitized signals that have already been sampled up to 4X or ~100 kHz. This will allow an RX5 to run a DSP chain at ~50 kHz or ~100 kHz, and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at a maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

When acquiring up to 16 channels of data on the first fiber optic input port of the RX5, the signals will be oversampled 4X to 100 kHz. If data is being acquired only on the first two fiber optic ports, the signals will be oversampled 2X to ~50 kHz.

Amp Status and Clip Warning Lights

Amp lights are located to the right of each fiber optic port. These lights are used to indicate the power status or provide a clip warning for the connected amplifiers.

When an amplifier is not connected the Amp light will flash in a slow steady pattern. The light is lit when the amplifier is connected and begins to flash quickly when the voltage on the battery for the corresponding amplifier is low. When any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier, the corresponding light will flash rapidly to warn that clipping may occur if the signal exceeds the maximum input voltage. See the corresponding preamplifier section for more information on input range and clip warnings.

Important! The Li-ion batteries voltage decreases rapidly once the battery low light is on. Data acquisition will suffer if the battery is not charged soon after the light goes on.

Amplifier Status Patterns

Light Pattern	Amplifier Status
Solid	Connected
Very slow flash (~1 every 2 seconds)	Not connected
Slow flash (~1 per second)	Connected and charging
Rapid flash	Battery low
Very rapid flash	Clip Warning

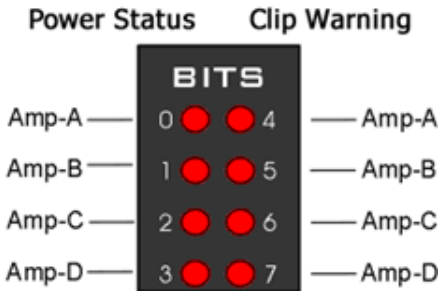
Note: If the amplifier appears to be connected and the amplifier status light is flashing slowly, check to ensure that the device is connected properly.

Bits Lights

The RX5's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (light when high) for the eight bit-addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as logic level lights for any of the other four bytes of digital I/O.

Using the Bits Lights to Display Amplifier Status

Note: Because clip warning and amplifier status are always displayed using the Amp lights (located directly to the right of each fiber optic port), **TDT recommends using the Bits lights for other applications.** See "Amp Status and Clip Warning Lights" on page 3-29 for more information.



When the Bits lights are configured to display the amplifier status, the left column of lights indicates the power status and the right column indicates a clip warning for the corresponding amplifier.

"Amplifier Status Patterns" on page 3-29 shows the light pattern and corresponding amplifier status for the power status lights (0 - 3). Clip lights flash very rapidly when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier.

Analog Output

The RX5 is equipped with four channels of 16-bit PCM D/A. The sampling rate is user selectable up to a maximum of ~100 kHz. The D/A is DC coupled and has a built-in upsampler for improved audio playback. The upsampler is controlled through one of the RX5's programmable bits and can be turned off to allow the D/A to drive external devices such as a stimulator. Channel one analog output can be accessed via a front Panel BNC (DAC-1). All four analog channels can be accessed via the DB25 Multi I/O connector (pins 14 – 17).

Digital I/O

The RX5 processor has 40 digital I/O lines. Eight bits are bit-addressable. The remaining 32 bits are four word-addressable bytes. Digital I/O lines are accessed via the two 25-pin connectors on the front of the RX5. See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

CAUTION!: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

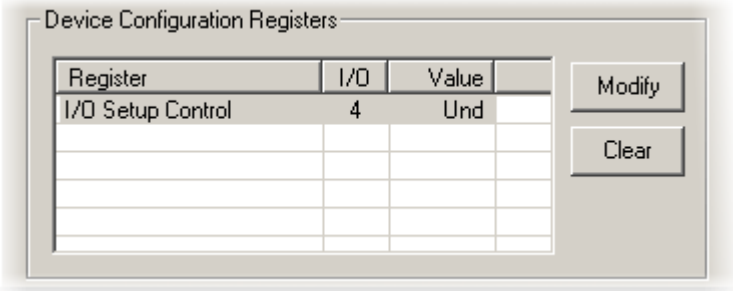
Each of the eight bit-addressable lines can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A, byte B, byte C, and byte D. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

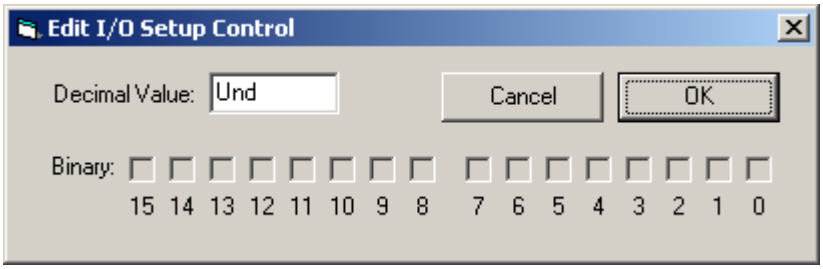
To access the bit configuration register in RPvdsEx:

1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Device Type** box and select the **RX5 Pentusa** from the list.

   The dialog expands to display the **Device Configuration Register**.



3. Click **Modify** to display the Edit I/O Setup Control dialog box.



In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.

4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.
6. When the co**nfiguration is complete, click OK to return to the** Set Hardware Parameters dialog box.

Bit_#	Description
0-7	Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output.
8-11	Each of these bits controls the configuration of one of the four addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 - byte A, bit 9 - byte B, bit 10 - byte C, and bit 11 - byte D
12-14	Create a bit code that determines how the front panel Bits lights are used, see table below.
15	Setting the bit to one will disable the D/A upsampler.

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 –14 in the Edit I/O Setup Control dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (lit when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

Bit Flags	Bits set to 1	Bit Lights Used For ...
000 	None	Logical level lights for bit-addressable I/O lines
010 	13	Amplifier Clip Warning/Power Status display
100 	14	Enable logical level lights for byte A
101 	12, 14	Enable logical level lights for byte B
110 	13, 14	Enable logical level lights for byte C
111 	12, 13, 14	Enable logical level lights for byte D

XLink

The XLink is not supported at this time.

RX5 Technical Specifications

Specifications for the A/D converters are found under the preamplifier's technical specifications.

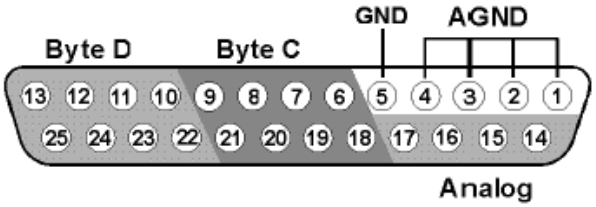
DSP	100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five
Memory	128 MB SDRAM (Shared)
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 97.65625 kHz (8X upsampled to 200 kHz default operation)
Frequency Response	DC - Nyquist (~1/2 sample rate)
Voltage Out	+/- 10.0 Volts
Voltage Out Accuracy	+/- 10%
S/N (typical)	84 dB (20 Hz to 25 KHz) 82 dB with upsampling disabled
THD (typical)	-77 dB for 1 kHz output at 5 Vrms -74 dB with upsampling disabled
Output Impedance	10 Ohm
Fiber Optic Ports	Two or Four Inputs (Medusa)
Digital I/O	40 bits programmable (8 bits bit-addressable and a 32 bit word, addressable as 4 bytes)

Note: zBus chasis (ZB1PS) required for power and communication.

DB25 Connector Pinouts

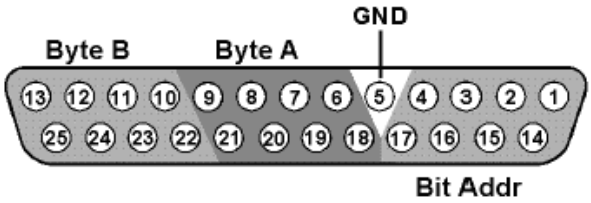
TDT recommends the PP24 patch panel for accessing the RX5 I/O.

Multi I/O



Pin	Name	Description		Pin	Name	Description
1	AGND	Analog Ground		14	A1	Analog Output Channels
2				15	A2	
3				16	A3	
4				17	A4	
5	GND	Digital I/O Ground		18	C0	Byte C Word addressable digital I/O Bits 0, 2, 4, and 6
6	C1	Byte C Word addressable digital I/O Bits 1, 3, 5, and 7		19	C2	
7	C3			20	C4	
8	C5			21	C6	
9	C7			22	D0	Byte D Word addressable digital I/O Bits 0, 2, 4, and 6
10	D1	Byte D Word addressable digital I/O Bits 1, 3, 5, and 7		23	D2	
11	D3			24	D4	
12	D5			25	D6	
13	D7					

Digital I/O



Pin	Name	Description		Pin	Name	Description
1	BA0	Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	BA1	Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	BA2			15	BA3	
3	BA4			16	BA5	
4	BA6			17	BA7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					