RX6 Multifunction Processor



RX6 Overview

The RX6 Multifunction Processor is a high performance multiple DSP device for researchers who need to acquire or produce high sample rate signals. The RX6 supports complex research, multimodal, and experimental paradigms on a single high-bandwidth device.

The RX6 equipped with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs, combines a powerful multiprocessor architecture and high-speed data transfer with two channels of 24-bit sigma-delta D/A converters and two channels of 24-bit sigma-delta A/D converters to provide superior high frequency signal generation and acquisition. Optionally, the RX6 can be equipped with a fiber optic input, allowing it to serve as a base station for a Medusa preamplifier.

Power and Communication

The RX6 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT runtime applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RX Architecture

Each RX multiprocessor device is equipped with either two or five digital signal processors (DSPs). The multi-DSP architecture allows processing tasks to be

distributed across multiple processors and enables data to be transferred to the PC quickly and efficiently. The DSPs include one master and one or four auxiliary DSP(s). 128 MB SDRAM of system memory is shared by all DSPs. When designing circuits the maximum number of components for each RX DSP is 256.

Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

Because the zBus communicates only with the master processor, these devices operate most efficiently when the circuit related processing tasks assigned to the master DSP are minimized, allowing more processor power (cycles) for communication and overhead tasks.



The RX6 contains a DB25 connector for interfacing with 24 bits of digital I/O and four BNC connectors for interfacing with four channels of analog I/O. An optional fiber optic Medusa preamp port enables connections for up to 16 channels of analog input.

Distributing Data Across DSPs

In RPvdsEx data can be transferred between each of the auxiliary DSPs as well as the master DSP using zHop components.





Components such as MCzHopIn and MCzHopOut can be used for multi-channel signals while components such as zHopIn, zHopOut, and MCzHopPick are used with single-channel signals. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop Bus introduces a single sample delay. However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX6 Features

DSP Status Displays

All high performance RX multiprocessors include status lights and a display screen to report the status of the individual processors.

Status Lights



Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash rapidly (\sim 3 times per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run! or Idle, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

| Cyc: | cycle usage |
|-------|---|
| Ovr: | processor cycle overages |
| Bus%: | percentage of internal device's bus capacity used |
| I/O%: | percentage of data transfer capacity used |

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Fiber Optic Port - Optional

The RX6 can include a single fiber optic port most often used with the HTI3, but may also be used to acquire digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier and the base station. The port can input up to 16 channels at a maximum sampling rate of ~25 kHz. See "Fiber Oversampling", below for more information. The fiber optic port can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A 1 - 16

Fiber Oversampling

The fiber optic cable that carries the signals to the fiber optic input ports has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sample rate of 24.414 kHz.

However, the need may arise to run a circuit at a higher sample rate while still acquiring data via a fiber optic port. The fiber optic port on the RX6 can oversample the digitized signals that have already been sampled up to 4X or ~100 kHz. This will allow an RX6 to run a DSP chain at ~50 kHz or ~100 kHz, and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at a maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~ 25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Amp Status and Clip Warning Lights

If the RX6 includes a fiber optic port for a Medusa Preamplifier, an Amp light is located to the right of the fiber optic port. This light is used to indicate the power status or provide a clip warning for the connected amplifier.

When an amplifier is not connected the Amp light will flash in a slow steady pattern. The light is lit when the amplifier is connected and begins to flash quickly when the voltage on the battery for the corresponding amplifier is low. When any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier, the corresponding light will flash rapidly to warn that clipping may occur if the signal exceeds the maximum input voltage. See the preamplifier user guide for more information on input range and clip warnings.

Important! The Li-ion batteries voltage decreases rapidly once the battery low light is on. Data acquisition will suffer if the battery is not charged soon after the light goes on.

| Light Pattern | Amplifier Status |
|--|------------------------|
| Solid | Connected |
| Very slow flash (~1 every two seconds) | Not connected |
| Slow flash (~1 per second) | Connected and charging |
| Rapid flash | Battery low |
| Very rapid flash | Clip Warning |

Amplifier Status Patterns

Note: If the amplifier appears to be connected and the amplifier status light is flashing slowly, check to ensure that the device is connected properly.

Bits Lights

The RX6's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (light when high) for the eight bit-addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as logic level lights for any of the other two bytes of digital I/O.

Using the Bits Lights to Display Amplifier Status

Note: Because clip warning and amplifier status are always displayed using the Amp lights (located directly to the right of each fiber optic port), **TDT recommends using the Bits lights for other applications.** See "Amp Status and Clip Warning Lights" on page 3-16 for more information.



When the Bits lights are configured to display the amplifier status, the left column of lights indicates the power status and the right column indicates a clip warning for the amplifier. The table above shows the light pattern and corresponding amplifier status for the power status lights (0-3). Clip lights flash very rapidly when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier.

Analog Input/Output

The RX6 has two channels of 24-bit, sigma-delta D/A and two channels of 24-bit, sigma-delta A/D, each accessible through BNC connectors. Sigma-delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. The RX6 DAC Delay is 43 samples and the RX6 ADC Delay is 70 samples.

This device can sample at rates up to ~ 260 kHz for a realizable bandwidth of ~ 109 kHz. For specific information on the actual sampling rates see "Realizable Sampling Rates for the RX6" on page 3-20.

Important! Because some RX6 models can acquire analog signals using a Medusa preamplifier via an optional fiber optic port, the sigma-delta A/D inputs on all RX6 models are offset and accessed as A channels 128 and 129.

Digital I/O

The RX6 processor includes 24 bits of programmable I/O in two eight bit wordaddressable bytes and eight bits of bit-addressable I/O. Digital I/O lines are accessed via the 25-pin connector on the front panel and can be configured as inputs or outputs.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

The first four bits of digital I/O (bits 0-3) can also be used for submicrosecond event timing. See the "TimeStamp" component in the *RPvdsEx Manual* for more information.

CAUTION !: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

Each of the eight bit-addressable bits can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A and byte B. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

To access the bit configuration register in RPvdsEx:

- 1. Click the Device Setup command on the Implement menu.
- 2. In the **Set Hardware Parameters** dialog box, click the Device Type box and select the RX6 Multi-Function from the list.

The dialog expands to display the Device Configuration Register.

| Register | 1/0 | Value | Modify |
|-------------------|-----|-------|--------|
| 1/O Setup Control | 4 | Und | |
| | | | Clear |
| | | | |

3. Click Modify to display the Edit I/O Setup Control dialog box.

| 🛢 Edit I/O Setup Control | × |
|---|-----------------|
| Decimal Value: Und | Cancel OK |
| Binary: F | 7 6 5 4 3 2 1 0 |

In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.

- 4. To enable the check boxes, delete Und from the Decimal Value box.
- 5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.
- 6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

| Bit_# | Description |
|-------|---|
| 0-7 | Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output. |
| 8-9 | Each of these bits controls the configuration of one of the two addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 controls byte A, and bit 9 controls byte B. |
| 10-11 | bits 10 - 11 are not used. |
| 12-14 | Create a bit code that determines how the front panel Bits lights are used, see table below. |
| 15 | Not used. |

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 -14 in the Edit I/O Setup Control dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (glow when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide

| Bit Flags | Bits set to 1 | Bit Lights Used For |
|---------------------------------|---------------|--|
| 000 | None | Logical level lights for bit-addressable I/O lines |
| 010 P P 14 13 12 | 13 | Amplifier Clip Warning/Power Status display |
| 100 F F F 14 13 12 | 14 | Enable logical level lights for byte A |
| 101 I I I 14 13 12 | 12, 14 | Enable logical level lights for byte B |

information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

XLink

The XLink is not supported at this time.

Realizable Sampling Rates for the RX6

The following table shows the actual sampling rate values for the RX6. The X's on the table correspond to realizable frequencies for the A, DAC, Optical input, and Digital I/O. For example, the Digital I/O accepts a sampling rate up to 390625.0 Hz and the Audio ADC and DAC each accept a sampling rate up to 260416.67 Hz. The maximum realizable sampling rates are accepted as the maximum sampling rate without distortion. Each of the inputs and outputs will function above these sampling rates, but distortion will be present in the signal.

| Standard Rate | Actual/Arbitrary Rate (Hz) | Audio A | Audio DAC | Optical/AMP Input | Digital I/O |
|------------------|-------------------------------|---------|-----------|----------------------|-------------|
| 6 kHz | 6103.52 | х | х | х | x |
| | 6975.45 | х | х | | x |
| | 8138.025 | х | х | | x |
| | 9765.63 | х | х | | x |
| 12 kHz | 12207.03 | х | х | х | x |
| | 13950.89 | x | х | | x |
| | 16276.04 | х | x | | x |

| Standard Rate | Actual/Arbitrary Rate (Hz) | Audio A | Audio DAC | Optical/AMP Input | Digital I/O |
|------------------|-------------------------------|---------|-----------|----------------------|-------------|
| | 19531.25 | x | x | | x |
| 25 kHz | 24414.06 | x | x | x | x |
| | 27901.79 | x | x | | x |
| | 32552.08 | x | x | | x |
| | 39062.50 | x | x | | x |
| 50 kHz | 48828.13 | x | x | X* | x |
| | 55803.57 | x | x | | x |
| | 65104.17 | x | x | | x |
| | 78125.00 | x | x | | x |
| 100 kHz | 97656.25 | x | x | X* | x |
| | 111607.14 | x | x | | x |
| | 130208.33 | x | x | | x |
| | 156250.00 | x | x | | x |
| 200 kHz | 195312.50 | x | x | | x |
| | 223214.29 | x | x | | x |
| | 260416.67 | x | x | | x |
| | 312500.00 | | | | x |
| 400 kHz | 390625.00 | | | | x |

| [x] = Fully functional | [x*] = Sampling | limited to 25KHz |
|------------------------|-----------------|------------------|
| [A] I any functional | [A] bumphing | |

RX6 Technical Specifications

The RX6 can be equipped with a fiber optic input port which may be used with a Medusa or Adjustable Gain preamplifier. Specifications for the AD converters of those devices are found under the preamplifier's technical specifications.

| DSP | 100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five |
|--------------------|--|
| Memory | 128 MB SDRAM |
| D/A | 2 channels, 24-bit sigma-delta |
| Sample Rate | Up to 260.4166 kHz |
| Frequency Response | DC - 109 kHz |
| Voltage Out | +/- 10.0 Volts |
| S/N (typical) | 105 dB (20 Hz - 20 kHz at 10 V) |

| THD (typical) | -92 dB (1 kHz output at 5 Vrms) | | |
|--------------------|---|--|--|
| Sample Delay | 43 samples | | |
| A/D | 2 channels, 24-bit sigma-delta | | |
| Sample Rate | Up to 260.4166 kHz | | |
| Frequency Response | DC – 109 kHz | | |
| Voltage In | +/- 10.0 Volts | | |
| S/N (typical) | 105 dB (20 Hz - 20 kHz at 10 V) | | |
| THD (typical) | -95 dB (1 kHz input at 5 Vrms) | | |
| Sample Delay | 70 samples | | |
| Fiber Optic Ports | Optional Input (Medusa) | | |
| Digital I/O | 24 bits programmable (8 bits addressable and a 16 bit word, addressable as 2 bytes) | | |
| Input Impedance | 10 kOhms | | |
| Output Impedance | 10 Ohms | | |

Note: zBus chasis (ZB1PS) required for power and communication.

Signal-to-Noise Ratio Diagram

The following graph is of the signal to noise ratio with varying signal frequencies.



dB Rolloff Diagram

This graph shows the dB rolloff for the RX6 with varying sampling frequencies for both D/A and A/D. The sample delay remains relatively stable for varying frequencies.



DB25 Connector Pinout

TDT recommends the PP24 patch panel for accessing the RX6 I/O.

Digital I/O



| Pin | Name | Description | | Pin | Name | Description |
|-----|------------|---|----|-----|-----------------------------|---|
| 1 | BAO | Bit Addressable digital I/O Bits 0, 2, 4, and 6 | | BA1 | Bit Addressable digital I/O | |
| 2 | BA2 | | | 15 | BA3 | Bits 1, 3, 5, and 7 |
| 3 | BA4 | | | 16 | BA5 | |
| 4 | BA6 | | 17 | 17 | BA7 | |
| 5 | GND | Digital I/O Ground | | 18 | A 0 | Byte A Word addressable digital I/ O Bits 0, 2, 4, and 6 |
| 6 | A1 | Byte A Word addressable digital I/ O Bits 1, 3, 5, and 7 | 19 | 19 | A2 | |
| 7 | A3 | | | 20 | A4 | |
| 8 | A5 | | | 21 | A6 | |
| 9 | A7 | | | 22 | BO Byte B | |
| 10 | B1 | Byte B Word addressable digital I/ O Bits 1, 3, 5, and 7 | | 23 | B2 | Word addressable digital I/ O Bits 0, 2, 4, and 6 |
| 11 | B 3 | | | 24 | B4 | |
| 12 | B5 | | | 25 | B 6 | |
| 13 | B7 | | | | • | • |