RZ2 BioAmp Processor

RZ2 Overview

The RZ2 BioAmp Processor has been designed for high channel count neurophysiology recording and signal processing. The RZ2 features two (RZ2-2), four (RZ2-4), or eight (RZ2-8) digital signal processors cards. Any card can be either a single standard processor card (RZDSP) or a quad-core processor card (QZDSP). Standard single processor cards use a single Sharc DSP; quad-core processor cards use four Sharc DSPs Cores with the potential to more than double the power of the RZ2. All cards are networked on a multiprocessor architecture that features efficient onboard communication and memory access. The highly optimized multi-bus architecture uses four dedicated data buses to eliminate data flow bottlenecks—all transparent to the user. This architecture yields an extremely powerful system capable of sophisticated real-time processing and simultaneous acquisition on all channels.

The RZ2 is typically used with a Z-Series Amplifier (such as the PZ5). High bandwidth data is streamed from the amplifier to the RZ2 over a lossless, fast, fiber optic connection. Both single and quad-core processors cards may include an optical interface for connection to devices such as the RS4 Data Streamer, an IZ2 Stimulator or a secondary PZ Amplifier. Each onboard optical connection can support 256 channels at sampling rates up to ~25 kHz and 128 channels at sampling rates up to ~50 kHz. The RZ2 also features 16 channels of analog I/O, 24 bits of digital I/O, two Legacy optical inputs for Medusa PreAmps, and an onboard LCD for system status display.

Power and Communication

The RZ2's Optibit optical interface ensures fast and reliable data transfer from the RZ2 to the PC and is integrated into the device. Connectors are provided on the back panel and are color coded for correct wiring. The RZ2's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

The RZ2 is UL compliant, see the *RZ2 Operations Manual* for power and safety information.

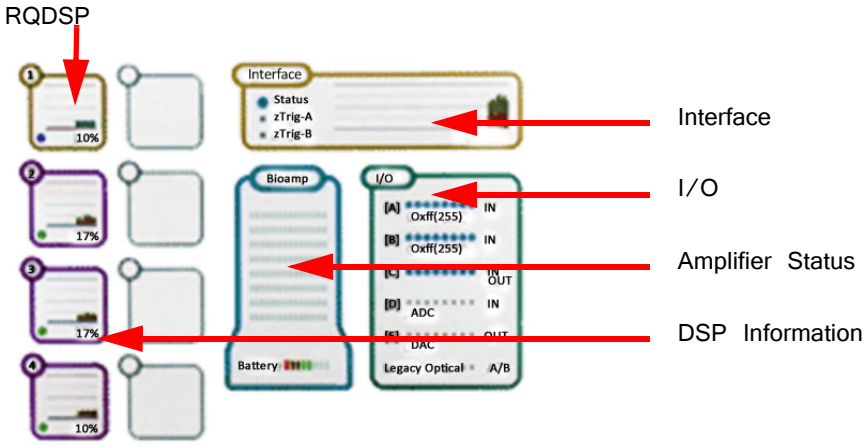
Software Control

TDT *Synapse* software controls the RZ2 and provides users a high level interface for device configuration.

Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed for designing circuits. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ2 TouchScreen

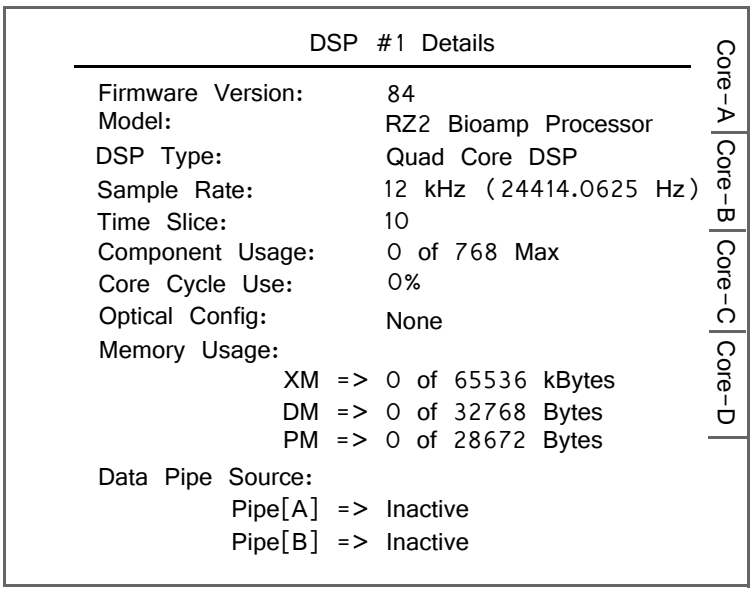
The touchscreen shows information about each DSP, the optical PC interface, a connected PZ preamplifier, and system I/O.



Touch a section of the screen to display more detailed information.

Screen Element	Information Displayed
DSPs	A stacked histogram shows cycle usage for each DSP with the bottom section (blue) showing the cycle usage taken up by circuit operation and the top section (pink) showing the cycle usage required for data transfer. If the cycle usage surpasses 100%, a bar is drawn above the 100% line in the cycle use histogram and will persist until the RZ2 is rebooted. For quad-core DSPs, the core with the highest cycle usage is displayed.

Touch to Display:



Optical Config is the peripheral device supported by the DSP, if any.

Data memory (DM) is the amount of DM used for filter delay line and short delays.

External Memory (XM) is the amount of XM used for long delays and buffers.

Program Memory (PM) is the amount of PM used to hold filter coefficients.

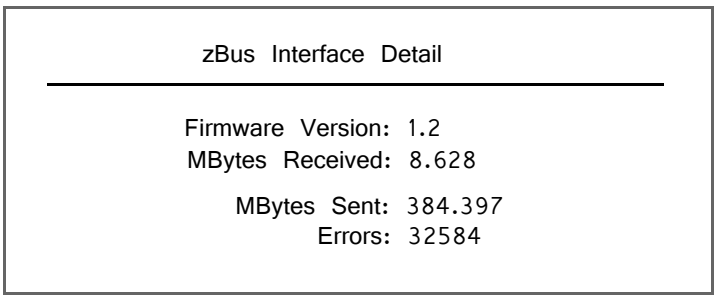
Tabs are enabled for quad-core DSPs, with one Core per tab.

Interface

Virtual Status lights display status of the interface (Status), zTrig-A, and zTrig-B. A stacked histogram shows data transfer rate in mb/s.

Touch to Display:

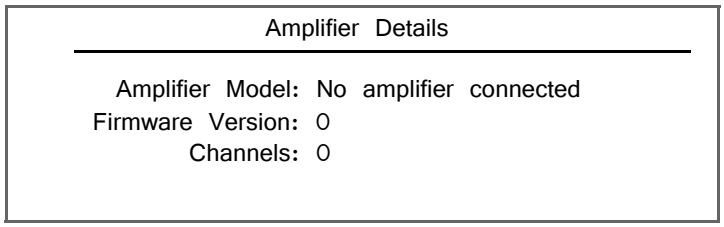
Firmware version, MB data received/sent and transfer errors.



Amp

Touch to Display:

Amp model, number of channels and firmware version of connected PZ series amplifier.



I/O Virtual indicator lights.

[A], [B], and [C]: Digital I/O

LED will light for an input bit or it will show the logic level for an output bit.

[D] and [E]: Analog I/O

16 lights indicate the signal level, green when a signal is present and red to warn that the signal is approaching the maximum voltage (at which point clipping would occur).

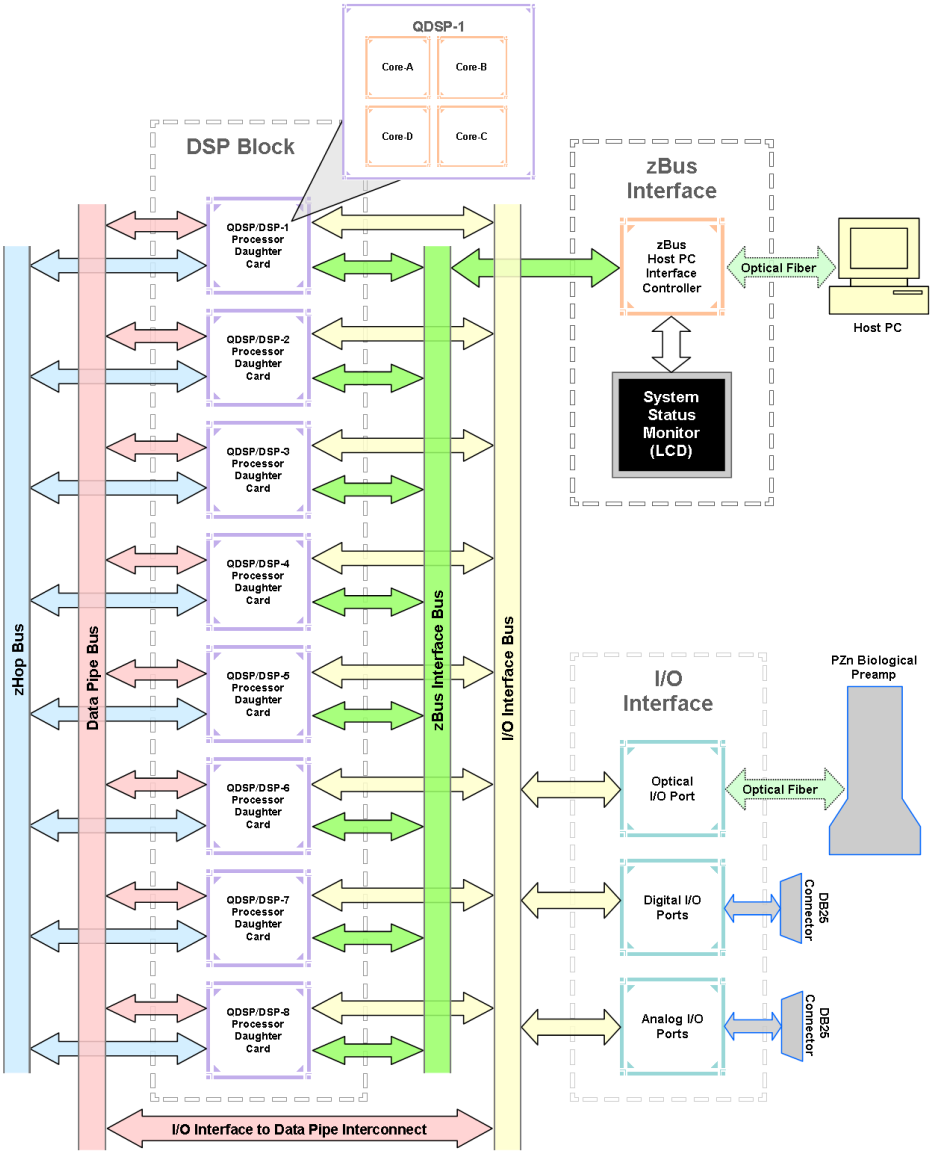
Legacy Optical: Amp Light For The Legacy Preamplifier Sync

Flashes yellow when no amp is connected and will be light green when the amplifier is correctly connected.

Note: Older versions of the RZ2 have a selection knob that allows the user to highlight a section of the screen. To display more detailed information, rotate the knob to select a system component and then push the knob to show the information view.

RZ2 Architecture

The RZ2 processor utilizes a highly optimized multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ2 Multi-DSP Architecture Functional Diagram

As shown in the diagram above, the RZ2 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to a local interface to the four data buses: two buses that connect each DSP to the other functional blocks and two that handle data transfer between the DSPs (as described further in Distributing Data Across DSPs below). Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such

as data buffers and filter coefficients) across processors. Memory use can be monitored on the RZ2 front panel display.

When designing circuits also note that the maximum number of components for each RZ2 standard RZDSP is 768 and 1000 for each QZDSP.

The zBus Interface The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus, allowing for large high-speed data reads and writes without interfering with other system processing.

The I/O Interface The I/O interface serves as a connection to outside signal sources or output devices. It is used primarily to input data from a PZ amplifier via the high speed optical port, but also serves the Legacy amplifier inputs and digital and analog channels. The I/O Interface Bus provides a direct connection to each DSP and the Data Pipe Bus.

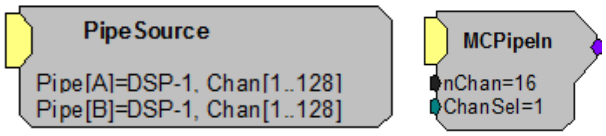
Distributing Data Across DSPs

For the best performance, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs. The RZ2 architecture provides three data buses for this type of data handling.

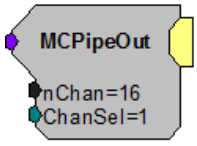
The Data Pipe Bus

The Data Pipe bus is optimized for handling high count multi-channel data streams and efficiently transfers up to 256 channels of data between DSPs. The Data Pipe bus also interconnects to the I/O Interface bus allowing direct access to data from the PZ amplifiers.

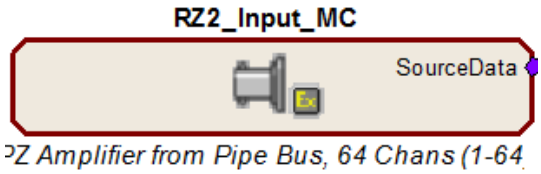
In RPvdsEx data can be transferred across the Data Pipe bus using Data Pipe components.



PipeSource and MCPipeIn components are used to select a data source (another DSP or the PZ amplifier) and feed data to a DSP circuit.



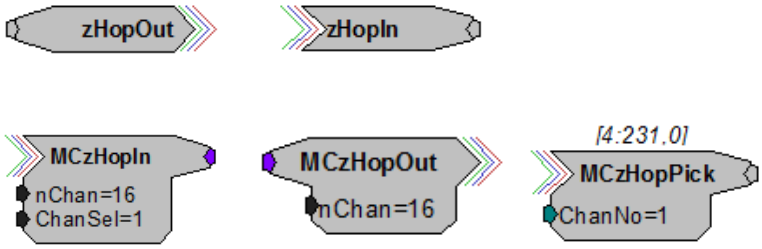
MCPipeOut feeds data off the DSP to the Data Pipe Bus.



The RZ2_Input_MC macro also transfers inputs from the I/O interface to the Data Pipe bus and DSPs.

The zHop Bus

The zHop bus is useful for transferring single or low channel count signals, such as timing and control signals.



In RPvdsEx data is transferred across the zHop Bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. These components can be used on any DSP or DSP-core. Up to 126 pairs can be used in a single RPvdsEx circuit.

The zHopBus is less efficient than the Data Pipe bus, so it is not recommended for multi-channel signals.

Bus Related Delays

A standard two sample delay is associated with the zHop, and Data Pipe. However, these delays are taken care of for the user in Synapse and when Timing and Data Saving macros are used in OpenEx.

50 kHz Sampling Rate Acquisition with the PZ Amplifier

The RZ2 and PZ amplifier support sample rates from ~6 kHz to ~50 kHz.

When sampling at a rate of ~50 kHz, there are several important considerations:

- Only the first 128 PZ amplifier channels will be available.
- All Data Pipes will have a max of 128 channels instead of 256.
- Both halves (A and B) of the PipeSource component must be selecting the desired source. For example, when acquiring data from a PZ amplifier, Pipe[A] and Pipe[B] both need to be set to Amp. Chan[1...128].

Data Transfer Rate

As with other devices, your expected sustained RZ-to-Host PC data rate should not exceed 1/2 to 2/3 of the rated data transfer speed. For the RZ2 device this is 160 Mbits/second (Mbps) so your designs should have a sustained data rate of no

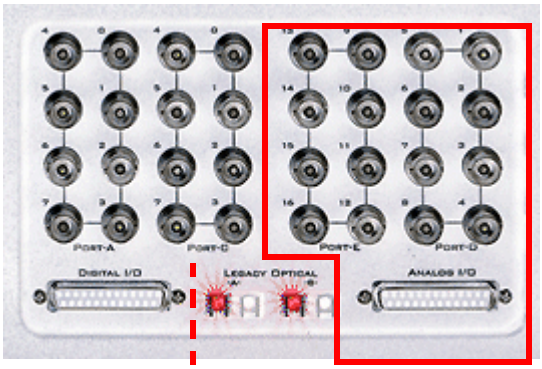
more than ~100 Mbps. When the RZ2 is processing, the current data transfer rate (Mbps) is displayed in the top right corner of the LCD Screen. This maximum rate may be further limited by your PC's ability to store the data to disk.

This equates to streaming a maximum of 160 channels at a sampling rate of ~25 kHz or 90 channels at a sampling rate of ~50 kHz. See "Calculating Data Transfer Rates" in the *OpenEx Manual* for more information.

RZ2 Features

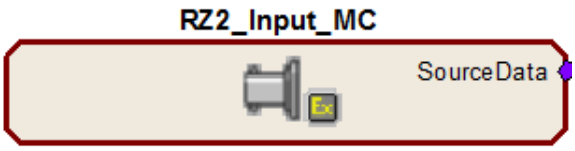
Amplifier and Onboard Analog I/O

The RZ2 is equipped with both optical port amplifier input and onboard analog I/O capabilities. The high speed fiber optic ports (located on the RZ2 back panel) and Legacy fiber optic ports allow a direct connection to Z-Series or Medusa preamplifiers. Physiological signals are digitized on the preamplifier and transferred across noiseless fiber optics.



Legacy PreAmp Input Analog I/O

The RZ2 also includes onboard D/A for stimulus generation and experiment control, and A/D for input of signals from a variety of other analog sources.



Data Pipe, 16 Chans (1-16)

The RZ2_Input_MC macro provides a universal solution for analog input via the RZ2, automatically selecting the correct components, applying any scale factors or channel offsets, and performing data type conversion needed based on information the user provides about the input source.

The table below provides a quick overview of these I/O features and how they must be accessed during circuit design. When the RZ2_Input_MC macro is not used, reference the table and be sure to use the appropriate component, channel offset,

scale factor and so forth. Further detail can be found below the table. Also, see the *RPvdsEx Manual* for more information.

Analog I/O	Description	Components	Chan.	Notes
Port D	Analog Input	AdcIn	1-8	Standard Configuration (may vary) Accessed through Port D BNCs or Analog I/O labeled DB25
Port E	Analog Output	DacOut	9-16	Standard Configuration (may vary) Accessed through Port E BNCs or Analog I/O labeled DB25
High Speed Fiber Optic Port	Z-Series BioAmp Input (located on RZ back panel)	MCPipeIn PipeIn recommended	1-256	When the RZ2_Input_MC is NOT USED, use MCInt2Float or Int2Float with a scale factor of 1e-9
		MCAdcIn	1-256	No scale required
Legacy Amp-A	Medusa PreAmp Input	AdcIn	17-32	When the RZ2_Input_MC is NOT USED, apply a scale factor of .000833
Legacy Amp-B	Medusa PreAmp Input	AdcIn	33-48	When the RZ2_Input_MC is NOT USED, apply a scale factor of .000833

Onboard Analog I/O

The RZ2 is equipped with eight channels of 16-bit PCM D/A and eight channels of 16-bit PCM A/D. All 16 channels can be accessed via front panel BNCs marked Port D and Port E or via a 25-pin analog I/O connector. See "RZ2 Technical Specifications" on page 1-14, for the DB25 pinout.

PZ Amplifier Fiber Optic Port

The RZ2's primary amplifier input, a high-speed fiber optic port is located on the back panel. The connectors on the fiber optic pair used for PZ amplifier communication are color coded for correct wiring. When designing circuits in RPvdsEx, the PZ amplifier input channels are accessed using the Pipe components. When the Data Pipe is used to feed signals from the amplifier an MCInt2Float or Int2Float must be used with a scale factor of 1e-9.

The amplifier inputs can also be accessed using the RPvdsEx MCAIn component starting at channel 1; however, this access method is less efficient and not recommended for high channel count applications. Unlike the Legacy Port, this high speed port can input up to 256 channels at a maximum sampling rate of 25 kHz or 128 channels at a maximum sampling rate of 50 kHz.

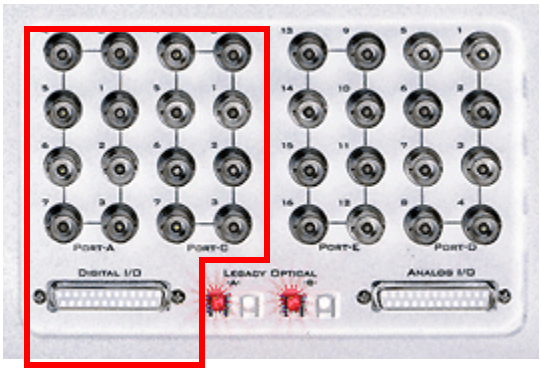
Legacy Fiber Optic Ports

The base station can also acquire digitized signals from the Medusa preamplifier, RA8GA, or other legacy enabled device over a fiber optic cable using the Legacy ports. Two Legacy fiber optic ports labeled -A- and -B- are provided to support simultaneous acquisition from up to two Medusa preamplifiers. Each port can input up

to 16 channels at a maximum sampling rate of 25 kHz. The Legacy fiber optic ports can be used with any of the Medusa preamplifiers including, the RA16PA, the RA4PA, or the RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Digital I/O

The digital I/O ports include 24 bits of programmable I/O. The digital I/O is divided into three ports (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ2 and ports A and C are available through BNC connectors on the front panel.



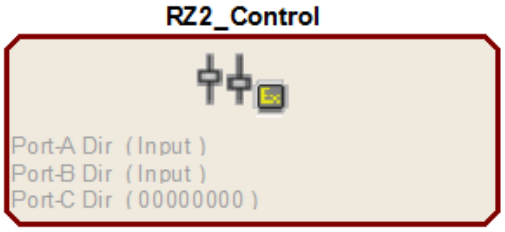
Digital I/O

See "RZ2 Technical Specifications" on page 1-14, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Port A	bits 0 - 7	Yes	Yes	byte addressable
Port B	bits 0 - 7	Yes	No	byte addressable
Port C	bits 0 - 7	Yes	Yes	bit addressable

The data direction for the Digital I/O is configured using the RZ2_Control macro in RPvdsEx.



Double-click the macro to access the settings on the Digital I/O tab. The RZ2_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ2_Control macro see the help provided in the macro's properties dialog box.

Note: For more information on addressing and Digital I/O see the *RPvdsEx Manual*.

The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. The table below depicts the different voltage outputs and thresholds for both types.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

UDP Ethernet Interface

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP RZ Communications Interface" on page 1-51, for more information.

Note: If the RZ2 has 4 optical DSP cards (see below) installed, the UDP Serial port is not available.

Specialized DSP/Optical Interface Boards (Optional)

The RZ standard DSP boards can be replaced with specialized DSP boards which include an optical interface for communication and control of RZ compatible devices, such as the IZ2 Stimulator and RS4 Data Streamer. RZ devices equipped with one or more specialized DSP boards include an optical port for each card. The ports are located on the back panel and labeled for easy identification.

RZDSP-I This board supports the IZ2 Stimulator, allowing the RZ device to function as a controller or base station. See "Software Control" on page 7-7, for more information on using and designing circuits for the stimulator.

RZDSP-S This board supports the RS4 Data Streamer, allowing the RZ device to stream data directly to the RS4's storage arrays. See "RS4 Data Streamer" on page 2-3, for more information on using and designing circuits for the streamer.

RZDSP-U This board supports the PO8e interface card, allowing the RZ device to stream data directly to storage arrays on a PC or other device. See "PO8e Interface for the RZ" on page 2-27, for more information.

RZDSP-P This board supports PZ amplifier input, providing an alternate method for acquiring data from a PZ amplifier. It can be used to expand the number of channels that can be acquired on any RZ processor. Access to this input can be enabled in the PZ control macro.

RZDSP-V This board supports the RV2 Video Tracking System, allowing the RZ device to function as a controller or base station. See "RV2 Video Processor" on page 8-3, for more information on using and designing circuits for the RV2.

QZDSP_OPT This version of the QZDSP quad-core processor includes an optical interface that can be programmed for use with any of the RZ compatible devices, such as a secondary PZ Amp, the IZ2 Stimulator, and RS4 Data Streamer. Core-A is always used for control of the peripheral device.

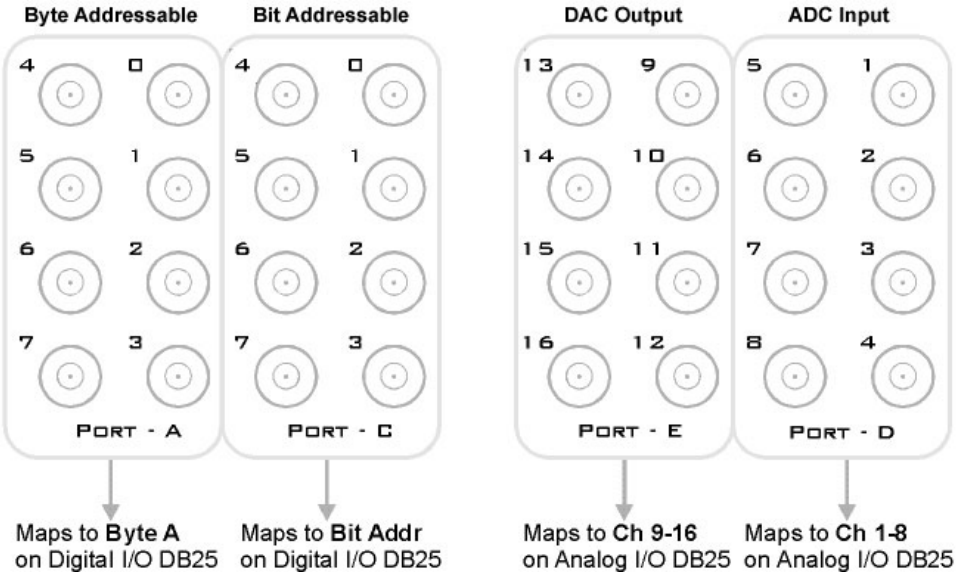
RZ2 Technical Specifications

Note: Technical specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

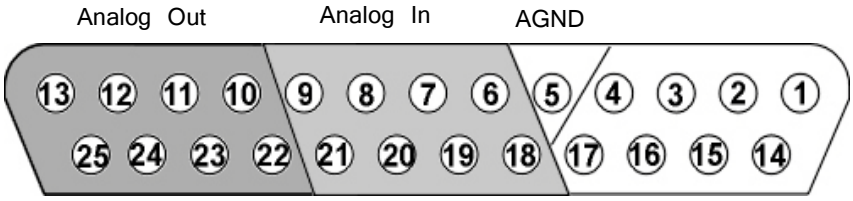
DSP	Up to eight standard and/or quad-core Standard: 400 MHz DSPs, 2.4 GFLOPS peak per DSP Quad-Core: Four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per core, four cores per QZDSP
D/A	8 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	8 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
Z-Series	One 256-channel input The maximum sample rate is 48828.125 Hz when recording up to 128 channels or 24414.0625 Hz when recording 129 - 256 channels).
Legacy (Medusa)	Two 16-channel inputs
Add-on Specialty (Optional)	Up to four, one per QZDSP_Opt or Specialty DSP card upgrade.
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top right block of BNCs for each port and is printed on the face of the device to minimize miswiring. The figure below represents the standard configuration and may vary depending on customer request.

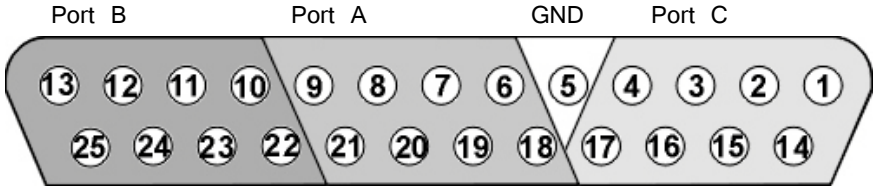


DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	A Analog Input Channels (Port D)
6	A2	A Analog Input Channels (Port D)		19	A3	
7	A4			20	A5	
8	A6			21	A7	
9	A8			22	A9	DAC Analog Output Channels (Port E)
10	A10	DAC Analog Output Channels (Port E)		23	A11	
11	A12			24	A13	
12	A14			25	A15	
13	A16					

DB25 Digital I/O Pinout



Pin	Name	Description	Pin	Name	Description
1	C0	Port C Bit Addressable Digital I/O Bits 0, 2, 4, and 6	14	C1	Port C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2		15	C3	
3	C4		16	C5	
4	C6		17	C7	
5	GND	Digital I/O Ground	18	A0	Port A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Port A Word Addressable Digital I/O Bits 1, 3, 5 and 7	19	A2	
7	A3		20	A4	
8	A5		21	A4	
9	A7		22	B0	Port B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Port B Word Addressable Digital I/O Bits 1, 3, 5 and 7	23	B2	
11	B3		24	B4	
12	B5		25	B6	
13	B7				