RZ5 BioAmp Processor

RZ5 Overview

The RZ5 BioAmp Processor is available with either one or two 400 MHz Sharc digital signal processors networked on a multiprocessor architecture that features efficient onboard communication and memory access. The optimized multi-DSP architecture provides nearly five gigaflops of processing power, making the RZ5 a versatile solution for real-time processing and simultaneous acquisition.

The RZ5 acquires and processes up to 32 channels of neurophysiological signals in real-time. Data can be input from two Medusa preamplifiers at a sampling rate of ~25 kHz. The RZ5 also supports microstimulation applications. The RZ5 can be used with one of TDT's stimulus isolators (MS16 or MS4) to comprise a complete microstimulation system. For more information, see "MS4/MS16 Stimulus Isolator" on page 7-33.

The RZ5 also features eight channels of analog I/O, 24 bits of digital I/O and an onboard monitor speaker with volume control.

Power and Communication

The RZ5's Optibit optical interface ensures fast and reliable data transfer from the RZ5 to the PC and is integrated into the device. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220V). If you need to change the voltage setting, please contact TDT support at 386.462.9622 or support@tdt.com.

The RZ5 is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

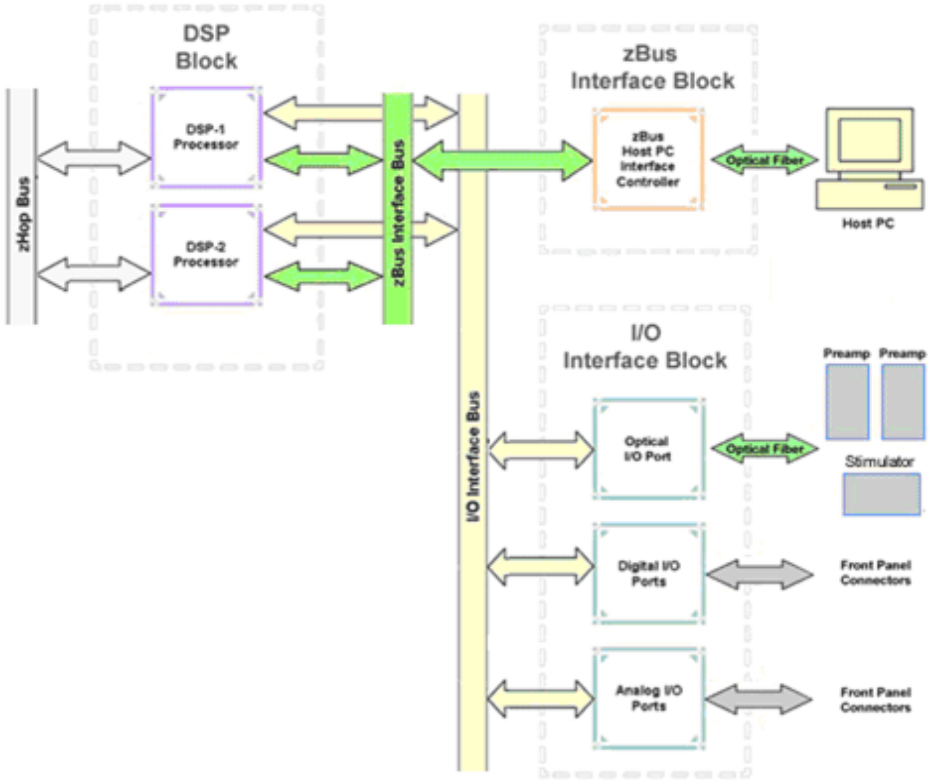
Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-

time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see "MultiProcessor Circuit Design" and "Multi-Channel Circuit Design" in the *RPvdsEx Manual*.

RZ5 Architecture

The RZ5 processor utilizes a multi-bus architecture and offers three dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



As shown in the diagram above, the RZ5 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to 64 MB SDRAM and a local interface to the three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (as described further in Distributing Data Across DSPs below). This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ5 DSP is 768.

The zBus Interface The zBus Interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus, allowing for large high-speed data reads and writes without interfering with other system processing.

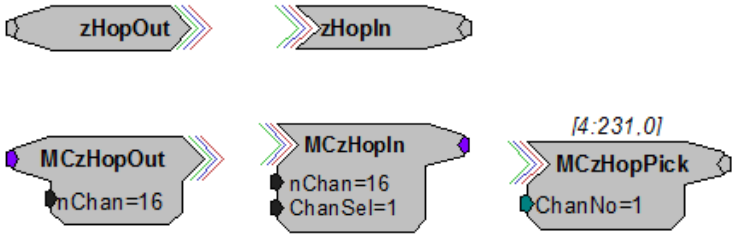
The I/O Interface The I/O Interface serves as a connection to outside signal sources or output devices. It is used to input data from the preamplifier inputs and digital and analog channels. The I/O Interface Bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To reap the benefits of added power made possible by multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs. The RZ5 architecture provides the zHop Bus for this type of data handling.

The zHop Bus

The zHop Bus allows the transfer of single or multi-channel signals between each DSP in the RZ5.



In RPvdsEx data is transferred across the zHop Bus using paired zHop Components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

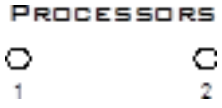
The zHop Bus introduces a single sample delay However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

RZ5 Features

DSP Status Displays

The RZ5 include status lights and a VFD (Vacuum Fluorescent Display) screen to report the status of the individual processors.

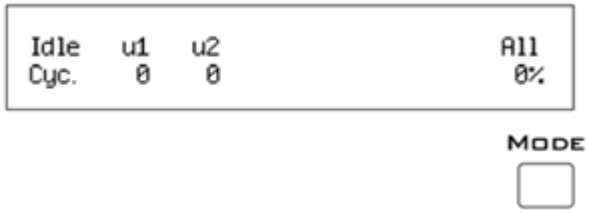
Status Lights



Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding

LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second).

Front Panel VFD Screen



The front panel VFD screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The VFD screen may also report system status such as booting status (Reset).

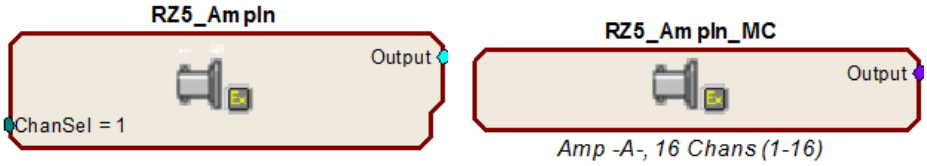
Note: When burning new microcode or if the firmware on the RZ5 is blank, the VFD screen will report a cycle usage of 99% and the processor status lights will flash red.

Status Indicators	Description
Cyc:	cycle usage (**note:** limited to 2 digits; ex: 110 displayed as 10)
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	Connection (sync) status of amplifiers A and B

Important! Status lights flash when a DSP goes over the cycle usage limit, even if only for a particular cycle. this helps identify periodic overages caused by components in time slices.

Amplifier and Onboard Analog I/O

The RZ5 is equipped with both amplifier input and onboard analog I/O capabilities. The fiber optic ports allow a direct connection to Medusa Preamplifiers. Physiological signals are digitized on the preamplifier and transferred across noiseless fiber optics. The RZ5_AmpIn_MC and RZ5_AmpIn macros automatically apply the necessary scale factors and channel offsets for configuring the preamplifier fiber optic ports.



The following table provides a quick overview of the amplifier and analog I/O features and how they must be accessed during circuit design. When the RZ5_AmpIn_MC and RZ5_AmpIn macros are not used, reference the table and be sure to use the appropriate component, channel offset, scale factor and so forth. Also, see the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Components	Chan.	Notes
A Inputs	Analog Input	AIn	1 - 4	Accessed through A Input BNCs or Analog I/O labeled DB25
DAC Outputs	Analog Output	DacOut	9 - 12	Accessed through DAC Output BNCs or Analog I/O labeled DB25
Optical Amp-A	Medusa PreAmp Input	AIn	17 - 32	When the RZ5_AmpIn_MC or RZ5_AmpIn is NOT USED, apply a scale factor of .000833
Optical Amp-B	Medusa PreAmp Input	AIn	33 - 48	When the RZ5_AmpIn_MC or RZ5_AmpIn is NOT USED, apply a scale factor of .000833

Onboard Analog I/O

The RZ5 is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked A and DAC or via a 25-pin analog I/O connector. See "RZ5 Technical Specifications" on page 1-59 for the DB25 pinout.

Fiber Optic Preamplifier Ports

The RZ5 acquires digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier(s) and the base station. Two fiber optic ports are provided to support simultaneous acquisition from up to two preamplifiers. Each port can input up to 16 channels at a maximum sampling rate of ~25 kHz.

The fiber optic ports can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A 17 – 32

Amp-B 33 – 48

Note: When using the RZ5_AmpIn_MC and RZ5_AmpIn macros, the necessary scale factors and channel offsets for configuring the fiber optic ports are automatically applied.

Fiber Oversampling (acquisition only)

The fiber optic cable that carries the signals to the fiber optic input ports on the RZ5 has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sampling rate of ~25 kHz.

However, the need may arise to run a circuit at a higher sampling rate while still acquiring data via a fiber optic port. The two fiber optic ports on the RZ5 can oversample the digitized signals that have already been sampled up to 2X or ~50 kHz. This will allow the RZ5 to run a DSP chain at ~50 kHz and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at its maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Fiber Optic Output (Stimulator) Port

The output port, labeled Stimulator, can be used to transfer microstimulation waveforms to the Stimulus Isolator and/or to control its digital output.

Important! This fiber optic port is disabled if the sampling rate of the system is set to a value greater than ~25 kHz.

Monitor Speaker

The RZ5 is equipped with an onboard speaker. To use the speaker feed the desired signal to output channel 9 using a DacOut component. The speaker is provided primarily for audio monitoring of a single channel of electrophysiological potentials during recording.

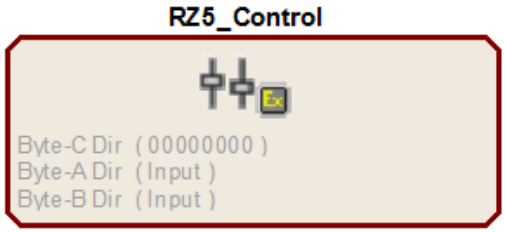
Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5 and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled Digital. See "RZ5 Technical Specifications" on page 1-59, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

The data direction for the Digital I/O is configured using the RZ5_Control macro in RPvdsEx.



Double-click the macro to access the settings on the Digital I/O tab. The RZ5_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ5_Control macro see the help provided in the macro's properties dialog box. For more information on addressing and "Digital I/O" see the *RPvdsEx Manual*.

Note: By default, all digital I/O are configured as inputs.

The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table depicting the different voltage outputs and thresholds for both type.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5 contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the VFD and DSP status LEDs and display information relative to the various analog and digital I/O contained on the RZ5. The following tables illustrate the possible display options and their associated descriptions.

Digital I/O - Byte C

8-bit, bit addressable byte C LED indicators are located to the bottom left of the RZ5 front panel.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O - A Inputs and DAC Outputs

A and DAC LED indicators are labeled and located to the right of the byte C LED indicators.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

Specialized DSP/Optical Interface Boards (Optional)

The RZ Standard DSP Boards can be replaced with specialized DSP Boards which include an optical interface for communication and control of RZ compatible devices, such as the IZ2 Stimulator and RV2 Video Processor. RZ devices equipped with one or more specialized DSP boards include an optical port for each card. The ports are located on the back panel and labeled for easy identification.

RZDSP-I This board supports the IZ2 Stimulator, allowing the RZ device to function as a controller or base station. See "Software Control" on page 7-10, for more information on using and designing circuits for the stimulator.

RZDSP-P This board supports PZ amplifier input, providing an alternate method for acquiring data from a PZ amplifier. It can be used to expand the number of channels that can be acquired on any RZ processor. Access to this input can be enabled in the PZ control macro.

RZDSP-V This board supports the RV2 Video Tracking System, allowing the RZ device to function as a controller or base station. See "RV2 Video Processor" on page 8-3, for more information on using and designing circuits for the RV2.

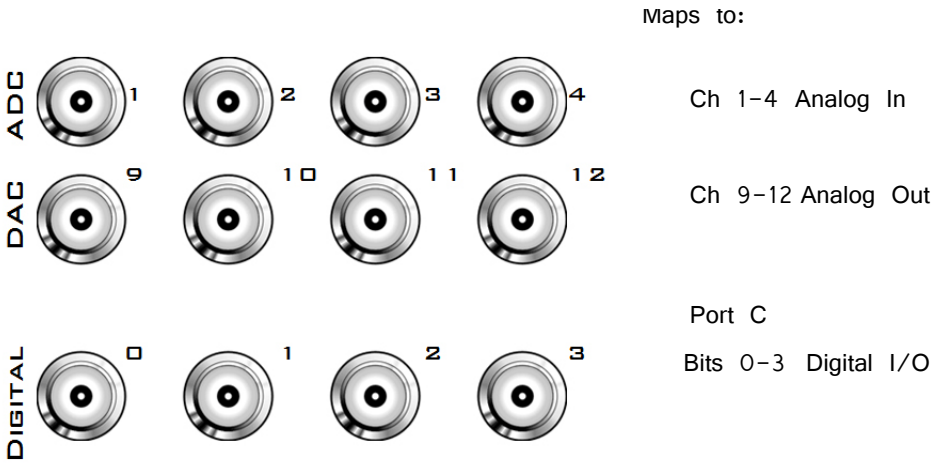
RZ5 Technical Specifications

Note: Technical Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

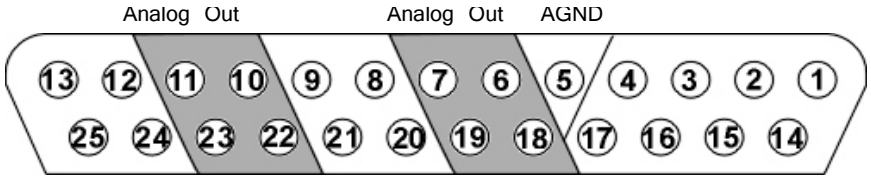
DSP	400 MHz DSPs, 2.4 GFLOPS peak per DSP One or Two
Memory	64 MB SDRAM per DSP
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz*
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz*
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
Stimulator (MS16)	One output for MS16 Stimulus Isolator When used with the Stimulus Isolator, the sampling rate is limited to 24.414 kHz.
Preamplifier (Medusa)	Two 16-channel inputs
Digital I/O	8 programmable bits: 3.3V, 25mA max load 2 programmable bytes(16 bits): 5.0 V, 35 mA max load
***The Stimulator fiber optic port is disabled if the sampling rate of the system is set to a value greater than ~25 kHz.**	

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.

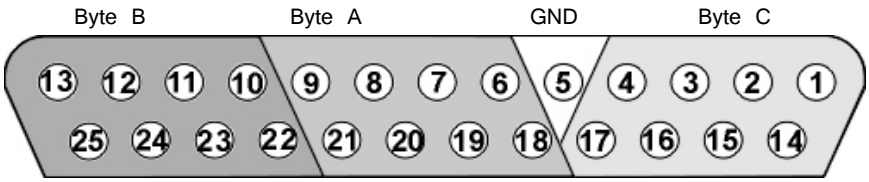


DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	ADC Analog Input Channels
6	A2	ADC Analog Input Channels		19	A3	
7	A4			20	NA	
8	NA			21	NA	
9	NA			22	A9	DAC Analog Output Channels
10	A10	DAC Analog Output Channels		23	A11	
11	A12			24	NA	
12	NA			25	NA	
13	NA					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A4	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					