RZ6 Multi I/O Processor

RZ6 Overview

The RZ6 Multi I/O Processor is a high sample rate processor with flexible input/output capabilities. The RZ6 features up to four digital signal processors cards; any card can be either a single standard processor card (RZDSP) or a quad-core processor card (QZDSP). Standard single processor cards use a single Sharc DSP, quad-core processor cards use four Sharc DSPs cores with the potential to more than double the power of the RZ6. All cards are networked in an optimized multiprocessor architecture that features efficient onboard communication and memory access. Two channels each of sigma-delta D/A and A/D converters provide a dynamic range of up to 115 dB and sampling rates up to ~200 kHz.

The single device form factor incorporates two channels of onboard programmable and manual attenuation and can drive headphones and standard, magnetic, or electrostatic speakers. It includes an onboard monitor speaker, two channels of amplification for analog inputs, and 24 channels of digital I/O. XLR, audio jack, and BNC connections are supported. Optionally, the RZ6 can be equipped with a fiber optic input, allowing it to support a four channel Medusa preamplifier.

The RZ6-A base version starts with a single DSP and makes an excellent all-in-one psychoacoustics system or can be added to any system to add audio stimulus generation to experiments.

The RZ6-A-P1 comes equipped with three DSPs for more processing power and includes the optional fiber optic input port, allowing it to serve as a BioAmp base station for ABR and OAE studies.

Both configurations can be upgraded with additional single or quad-core DSP cards (up to a maximum of four DSP cards) for complex filtering and high frequency applications.

Power and Communication

The RZ6's Optibit optical interface ensures fast and reliable data transfer from the RZ6 to the PC and is integrated into the device. Connectors are provided on the back panel and are color coded for correct wiring. The RZ6's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at 386.462.9622 or email support@tdt.com.

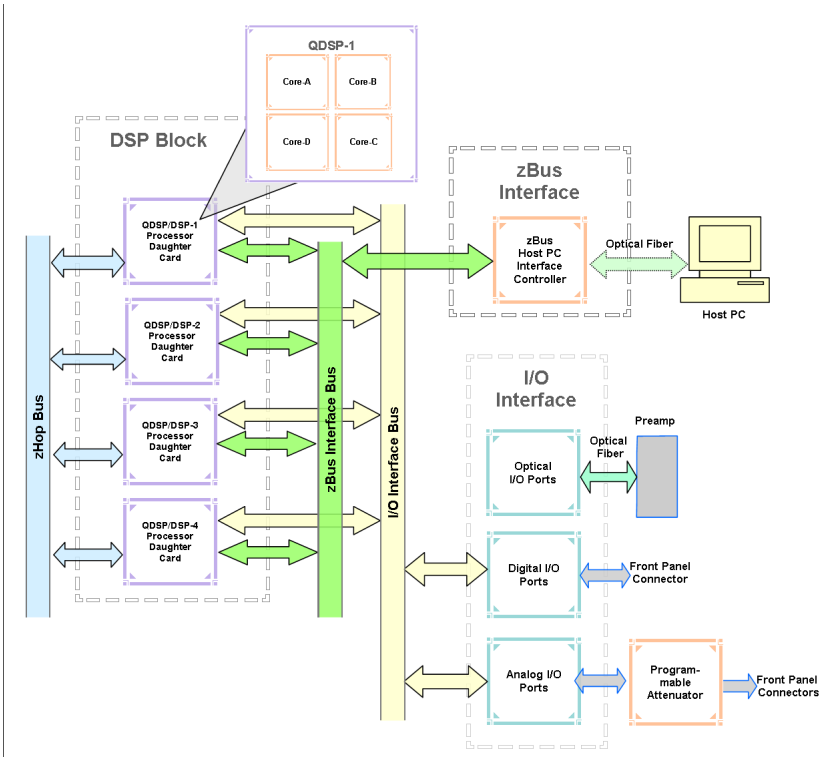
The RZ6 is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

Software Control

TDT Synapse or BioSigRZ software controls the RZ6 and provides users a high level interface for device configuration. Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. Several RZ6 macros are provided and are required to handle all programmable features related to the RZ6. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ6 Multi-Bus Architecture

The RZ6 processor utilizes a multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ6 Architecture Diagram

As shown in the diagram above, the RZ6 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP block is connected to three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (the zHop Bus). This architecture facilitates fast DSP-to-off-chip data handling.

Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. Large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ6 standard RZDSP is 768 and 1000 for each QZDSP.

The zBus Interface

The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus.

The I/O Interface

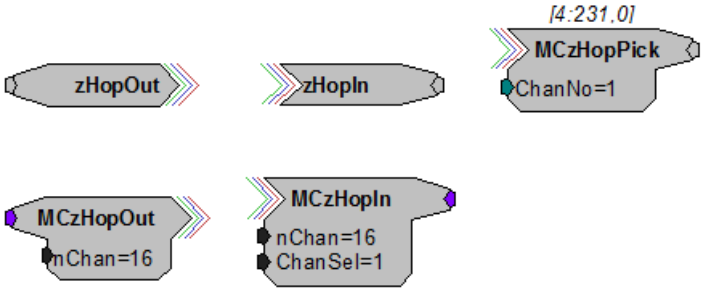
The I/O interface serves as a connection to outside signal sources or output devices. It is used to input data from the optional preamplifier input and digital and analog channels. The I/O interface bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To take advantage of multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs (or among cores of a quad-core DSP). The RZ6 architecture provides the zHop bus for transferring data across DSPs.

The zHop Bus

The zHop bus allows the transfer of single or multi-channel signals between each DSP in the RZ6.



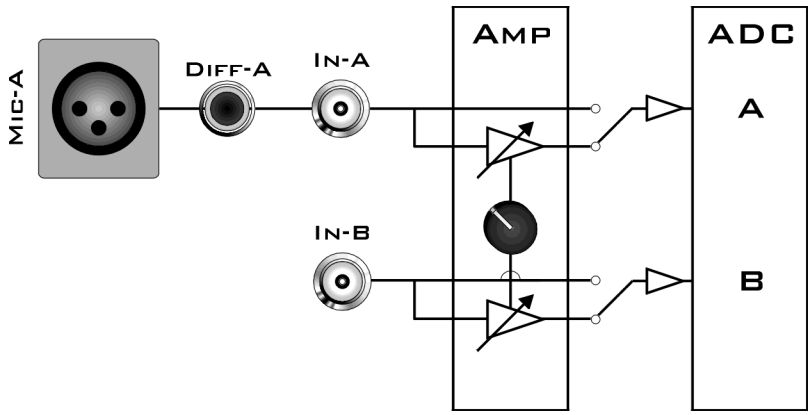
In RPvdsEx, data is transferred across the zHop bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit. **Bus Related Delays**

The zHop Bus introduces a two sample delay. This delay is taken care of for the user in Synapse, BiosigRZ, and in OpenEx (when Timing and Data Saving macros are used).

Functional Signal Flow Diagrams

The following diagrams illustrate how analog signals for channels A and B flow through the RZ6 and its modules. For more information on analog input and output see "Onboard Analog I/O and Optional Amplifier Input" on page 1-39.

The diagram to the below depicts the analog input flow for the RZ6.

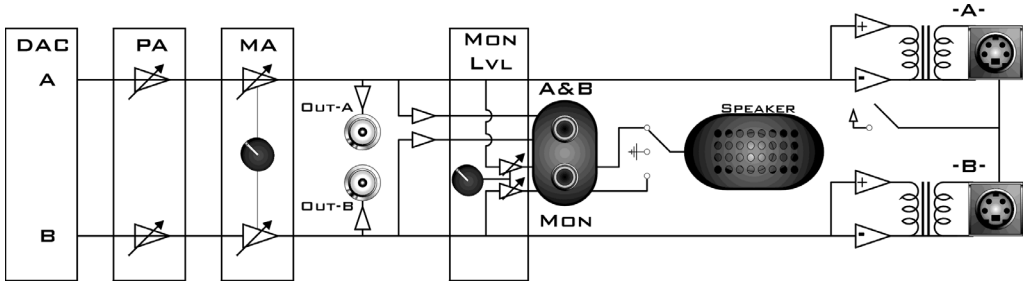


RZ6 Analog Input Flow Diagram

Input signals for channel A are input either through the XLR input (Mic-A), the audio jack input (Diff-A), or BNC (In-A). Input signals for channel B are input through the BNC (In-B).

A switch located to the left of the gain control knob allows a single gain setting for both channels to be applied or bypassed completely.

The diagram below depicts analog output flow through the RZ6.



RZ6 Analog Output Flow Diagram

Signals A and B flow out of the DAC and pass through the programmable and manual attenuation modules prior to being output on the front panel BNC connectors (Out-A and Out-B).

The signals for channels A and B are also passed to two stereo headphone output ports labeled A&B and Mon. Individual stereo power amplifiers are used for the BNC and stereo headphone outputs.

A single channel monitor speaker is connected either to signal A, signal B, or disabled based on the monitor control switch setting. The monitor level knob controls the sound level of both the stereo headphone jack labeled Mon and the monitor speaker.

Finally, if the electrostatic speaker driver is enabled via its switch, located on the front panel, signals A and B are output from the mini-DIN ports located on the RZ6 front panel.

RZ6 Features

Onboard Analog I/O and Optional Amplifier Input

The RZ6 is equipped with onboard analog I/O and may also include a fiber optic port for Medusa preamplifier input.

The following table provides a quick overview of the analog I/O and amplifier input features and how they must be accessed during circuit design. The RZ6 relies exclusively on macros for configuring analog and digital I/O and its fiber optic input port. See the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Channels	Required Macro
A Inputs	Analog Input	A and B	RZ6_AudioIn
DAC Outputs	Analog Output	A and B	RZ6_AudioOut
Optical Amp	Medusa PreAmp Input	1-4	RZ6_AmpIn

Onboard Analog Inputs

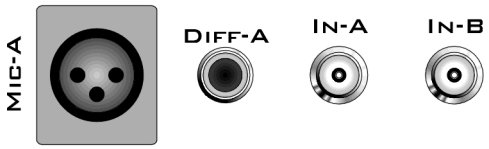
The RZ6 is equipped with two channels of 24-bit sigma-delta A/D converters. See "RZ6 Multi I/O Technical Specifications" on page 1-45, for more information.

Analog signals can be input through several connectors on the RZ6 front panel.

Channel A has three possible sources:

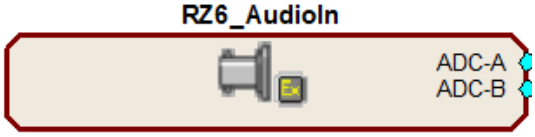
- MIC-A (XLR microphone input)
- DIFF-A (1/4" TRS microphone input)
- BNC labeled In-A

Channel B uses only the BNC labeled In-B:



Important! Use only one input for channel A at a time. Attempting to input signals from multiple sources will produce an erroneous signal.

Analog input is accessed in RPvdsEx through the RZ6_AudioIn macro.



A and B Microphone Amplifier

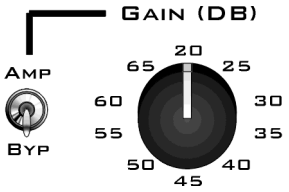
An onboard two channel amplifier provides gain for the onboard analog input signals (MIC-A, DIFF-A, In-A, and In-B). The switch located to the left of the gain control knob allows the current gain setting to be applied (if set to Amp) or bypassed completely (if set to Byp).

Important! When the gain is enabled, analog input signals MIC-A and DIFF-A are differential. Since the differential signals are summed a signal gain of 6 dB will be inherently applied. If the amplifier is bypassed, common mode rejection is disabled.

Note: To prevent clipping caused by a DC offset, the amplifier is AC coupled when the gain amplification is in use.

Gain

The front panel gain control knob can be used to the control overall signal level of both channels from 20 to 65 dB in 5 dB steps.



Fiber Optic Port - Optional

The RZ6-A-P1 acquires digitized signals from a Medusa preamplifier over a fiber optic cable. The port can be used with the RA4PA to input up to 4 channels.

Input from the preamplifier fiber optic port is accessed using the RZ6_AmpIn macro.

The fiber optic port (devices with serial number 1007 and greater) can also support the HTI3 Head Tracker Interface.

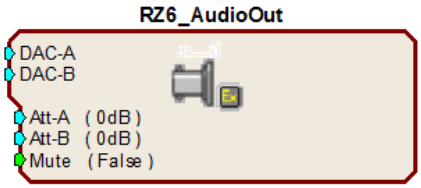
Fiber Oversampling (acquisition only)

Signals are digitized on the Medusa preamplifier at a maximum sampling rate of ~25 kHz, however, the fiber optic port on the RZ6 can oversample the digitized signals up to 8X or ~200 kHz. This will allow the RZ6 to run a DSP chain at ~200 kHz and still sample data acquired through an optically connected preamplifier.

Oversampling is performed on the RZ6. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Onboard Analog Outputs

The RZ6 is equipped with two channels of 24-bit sigma-delta D/A converters (see "RZ6 Multi I/O Technical Specifications" on page 45). Analog signals are output through a variety of connectors on the RZ6 front panel. Analog output is configured in RPvdsEx through the RZ6_AudioOut macro.



Programmable Attenuation

The RZ6_AudioOut macro provides access to two channels of programmable attenuation for precision control of analog output signal levels over a wide dynamic range.

Programmable attenuation in the RZ6 is achieved using both analog and digital attenuation methods. The device supports analog attenuation values of 0, 20, 40, and 60 dB. Attenuation values which lie in-between or exceed 60 dB are handled using digital attenuation.

For example, if you set an attenuation value of 66 dB in the RZ6_AudioOut macro, the analog attenuator will be set to 60 dB and the remaining 6 dB of attenuation will be applied by scaling the digital signal through RPvdsEx.

Note: For the best results, you should utilize the maximum D/A voltage range and use the RZ6_AudioOut macro to configure the desired attenuation setting for channels A and B.

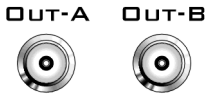
Manual Attenuator

The RZ6 includes another level of analog attenuation that can be controlled manually via the attenuator control knob from 0 to 27 dB in increments of 3 dB.

Manual attenuation is applied to both channels before the signals are output on any of the front panel connectors and is therefore applied in addition to any programmable attenuation set in RPvdsEx through the RZ6_AudioOut macro.

Analog Output via BNCs

DAC channels A and B are output to BNCs labeled Out-A and Out-B after attenuation has been applied. These outputs use a stereo power amplifier to drive TDT's MF1 multi-function speakers.



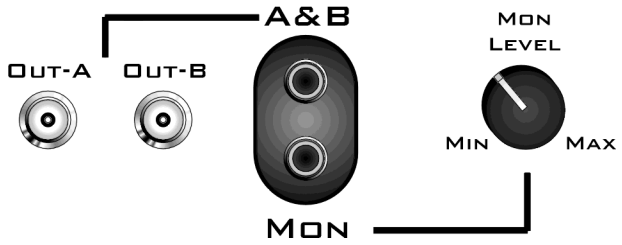
Note: A single signal generated or input from any of the RZ6 analog inputs can be ganged to reduce the spectral variation in power of the transducer across all frequencies (see "D/A Power Output Diagram" on page 1-47). To do this, configure your signal to output from both DAC channels as shown in the following diagram.

Ganged Output Connection Diagram

Configure your RPvdsEx circuit to output the same signal to DAC channels A and B then connect the transducer as shown in the diagram above.

Stereo Headphone Output

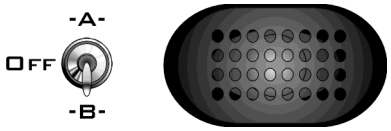
DAC channels A and B are also available as a stereo headphone output through two 1/8" audio jack connector ports (channel A is the left stereo output and channel B is the right stereo output). The port labeled A&B (top) provides a stereo headphone output suitable for experimental paradigms while the port labeled Mon (bottom) can be controlled by the Mon Level knob located directly to the right, making it more suitable for monitoring the experiment.



Audio Outputs

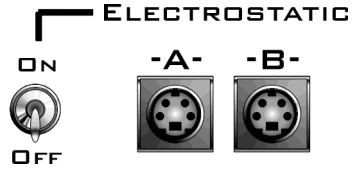
Note: All outputs use stereo power amplifiers

Monitor Speaker



The RZ6 is equipped with an onboard monitor speaker, provided for audio monitoring of a single channel. A switch located directly to the left of the monitor speaker is used to select between DAC channels A and B or to disable the monitor speaker. The monitor speaker output level is controlled by the Mon Level knob located directly to the right of the monitor stereo output.

Electrostatic Speaker Output



An onboard two channel broadband electrostatic speaker driver is provided, allowing direct connection of TDT's ES series electrostatic speakers. The driver produces flat frequency responses reaching far into the ultrasonic range, can drive two ES series speakers, and is powered using the onboard power supply. A switch located directly to the left of the two 4-pin, mini-DIN connectors is used to enable or disable output of DAC channels A and B.

Note: The electrostatic speaker driver is designed to work exclusively with TDT's electrostatic series speakers. Do NOT attempt to use any other speaker.

Important! If the electrostatic speaker driver is not being used, make sure that the ON/OFF switch is in the OFF position to reduce noise on the RZ6.

Digital I/O

Current RZ6 models are equipped with 24 bits of programmable digital I/O divided into three bytes (A, B, and C) as described in the chart below. Earlier versions

(serial number < 2000) were limited to 8 bits. By default, all lines are configured as inputs.

Data direction is configured using the RZ6_Control macro in RPvdsEx and may be controlled dynamically through the macro input port. For more information on using the RZ6_Control macro see the help provided in the macro's properties dialog box.

Digital I/O	Description	Notes
Byte A	bits 0 - 7	byte addressable
Byte B	bits 0 - 7	byte addressable
Byte C	bits 0 – 7	bit addressable

The Digital I/O connector can be found on the front of the RZ6. See "RZ6 Multi I/O Technical Specifications" on page 1-45, for pinout.

Voltage outputs and logic thresholds vary by type as shown in the table below.

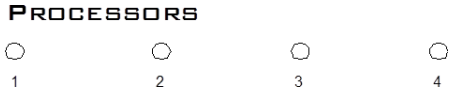
Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

See "Working with BitIn - BitOut" in the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming and addressing Byte C of the digital I/O. See "Working with WordIn -WordOut" in the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming and addressing Bytes A and B of the digital I/O.

DSP Status Displays

The RZ6 includes status lights and a VFD (Vacuum Fluorescent Display) screen to report the status of the individual processors.

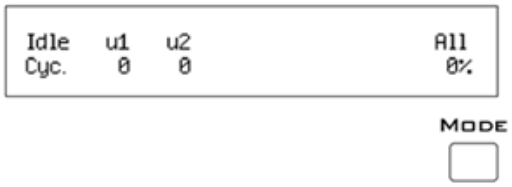
Status Lights



LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second). For QZDSPs, the LED represents the highest core cycle usage.

Important! The status lights flash when a DSP goes over the cycle usage limit, even if only for a cycle. This helps identify periodic overages caused by components in time slices.

Front Panel VFD Screen



The front panel VFD screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The VFD screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ6 is blank, the VFD screen will report a cycle usage of 99% and the processor status lights flashes red.

Status Indicators

Cyc:	cycle usage; for QZDSPs, the highest core cycle usage is shown **Note:** limited to 2 digits; ex: 110 displayed as 10.
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
DAC:	Displays the current analog attenuator setting. Also displays bars according to the RMS level of DAC A and B using a logarithmic scale. **Note:** Eight solid bars denote that the signal on DAC A or B is clipping.
A:	Displays bars according to the RMS Level on A A and B using a logarithmic scale. **Note:** Eight solid bars denote that the signal on A A or B is clipping.

Analog Input – A LED Indicators

The A LED indicators are labeled and located at the top right of the RZ6 front panel. The LEDs indicate the level of the signals on A channels A and B. This provides a useful indicator for adjusting the gain and to detect and prevent clipping. The following table describes the LED indicators' operation.

Light Pattern	LEDs Lit	Description
A B -6DB -12 -25 -50 LEVEL	4	Input is ≤ -6 dB down from max input voltage
	3	Input is between -6 dB and -12 dB down from max input voltage
	2	Input is between -12 dB and -25 dB down from max input voltage
	1	Input is between -25 dB and -50 dB down from max input voltage

Digital I/O LED Indicators

The digital I/O LED indicators are located directly below the VFD and DSP status LEDs and display information relative to the digital I/O contained on the RZ6. There are 8 LEDs one for each bit addressable digital I/O channel (Byte C). Each LED may display one of four states. The following table illustrates the possible display options and their associated descriptions.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog Input - Fiber Optic Port LED Indicator

A single green LED indicator is provided for the fiber optic input port on the RZ6-A-P1. When lit the LED signifies a Medusa preamplifier is correctly synced with the RZ6.

RZ6 Multi I/O Technical Specifications

Note: The RZ6 can be equipped with a fiber optic input port and used with a four channel Medusa preamplifier. See the preamplifier's technical specifications for A/D converters.

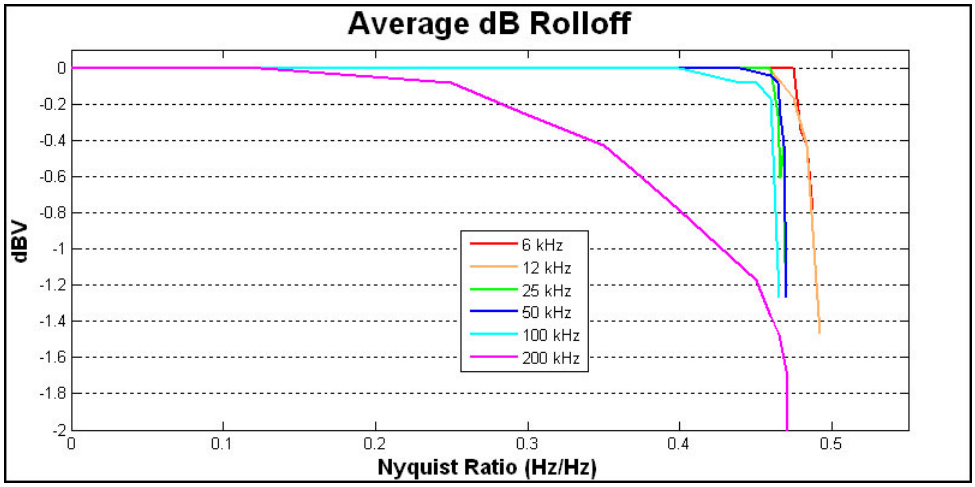
DSP	Up to four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per QZDSP core
D/A	2 channels, 24-bit sigma-delta
Sample Rate	Up to 195312.50 Hz
Frequency Response	DC - 0.44*Fs (Fs=sample rate)

Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	115 dB (20 Hz - 80 kHz at 5 Vrms)
THD (typical)	-90 dB (1 kHz output at 5 Vrms)
Sample Delay	31 (Serial numbers > 2000) 47 (Serial numbers < 2000)
A/D	2 channels, 24-bit sigma-delta
Sample Rate	Up to 195312.50 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage In	+/- 10.0 Volts
S/N (typical)	115 dB (20 Hz - 80 kHz at 5 Vrms)
THD (typical)	-90 dB (1 kHz output at 5 Vrms)
Sample Delay	66 samples
Fiber Optic Ports	**Optional Input Available on RZ6-A-P1 only** Supports 4-channel Medusa preamplifier or HTI3 Head Tracker Interface (serial number 1007 and greater)
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load
A and B Microphone Amplifier	Single setting for both channels (AC coupled when enabled)
High Pass Corner Frequency	3.6 Hz (Active only if the Amplifier is enabled)
Gain Settings	20 to 65 dB
Gain Step Size	5 dB
Programmable Attenuation	2 channels
Switching Time	1 sample
Settling Time	3 µsec
Transient Voltage	~370 mV
Hardware Attenuation Settings	0, 20, 40, 60 dB
Manual Attenuation	Single setting for both channels
Attenuation Settings	0 to 27 dB
Attenuation Step Size	3 dB
Amplification	2 channels
Spectral Variation	< 0.1 dB from 50 Hz to 200 kHz

Signal Noise	115 dB (20 Hz to 80 kHz)
THD	< 0.02% at 1 Watt from 50 Hz to 100 kHz
Noise Floor	20 µV rms
Input Impedance	10 kOhm
Output Impedance	1 Ohm 0.5 Ohm ganged
Headphone Output	2 channels
Output Impedance	1 Ohm
Electrostatic Speaker Output	2 channels Note: For further information on speaker specifications, "EC1 Technical Specifications" on page 16-12.

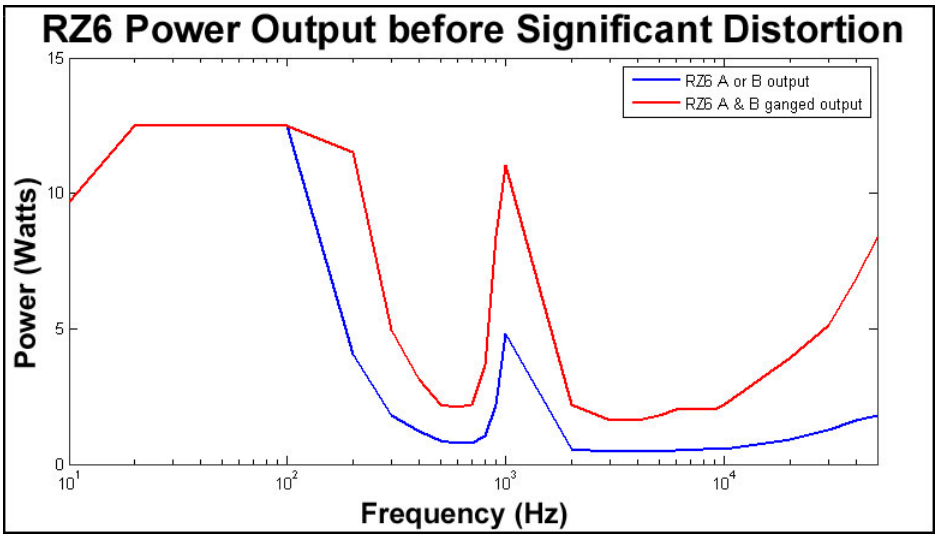
D/A dB Rolloff Diagram

This graph shows the dB rolloff for the RZ6 with varying sampling frequencies for the D/A. The sample delay remains constant for varying frequencies.

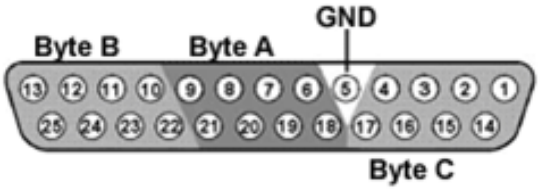


D/A Power Output Diagram

This graph shows the power output for the RZ6 with varying driving frequencies for the D/As when driving a four Ohm load. Driving higher impedance loads will reduce spectral variation.

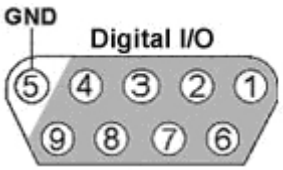


DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

Digital I/O – DB9 Connector Pinout



Note: Serial numbers < 2000 only.

Pins	Name	Description		Pin	Name	Description
1	D0	Digital I/O 0, 2, 4, 6		5	GND	Ground
2	D2			6	D1	Digital I/O bits 1, 2, 3, 5, 7
3	D4			7	D3	
4	D6			8	D5	
5	GND	Ground		9	D7	